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09/316,699	05/21/1999	WILLIAM J. DALLY	AVI99-01	8189

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EXAMINER	
LY, ANH VU H	

ART UNIT	PAPER NUMBER
2667	19

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/316,699	Applicant(s) DALLY ET AL.	
	Examiner Anh-Vu H Ly	Art Unit 2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28 and 30-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 30-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to applicant's amendment filed March 22, 2004. Claims 1-28 and 30-56 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 8-19, 23-34, 36-42, and 44-56 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Kadambi et al (US Pub No. 2002/0093974 A1) in view of Ben-Michael et al (EP O 886454A2) and further in view of Brant et al (US Patent No. 5,805,787). Hereinafter, referred to as Kadambi, Ben-Michael and Brant.

With respect to claims 1, 16, 31, 40, and 46-49, Kadambi discloses (page 4, paragraphs 44-45, page 19, paragraphs 217-221, and Fig. 2) that the common buffer memory pool or CBP 50 is first level high speed SRAM memory, packet memory cache, for storing the received data packets and considered as on-chip data memory (a first set of rapidly accessible buffers, operating as a cache, which store information units received at an input link). Further, Kadambi discloses that global memory buffer pool or GBP 60 acts as a second level memory and is located off-chip. Since, the GBP 60 is an off-chip memory therefore it is slower to access than the CBP 50 (a second set of buffers for the information units that are accessed more slowly that

the first set). Kadambi does not disclose the information units from the first set of buffers being evicted to second set of buffers. Ben-Michael discloses in Fig. 7, a block diagram illustrating on-chip memory and off-chip memory for storing data packets in a network switch or router, wherein, the data packets being evicted from the on-chip memory to the off-chip memory when the on-chip memory is full. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the feature of storing the data packets in the on-chip memory and transferring the data packets to the off-chip memory when the on-chip memory is full in Kadambi's system, as suggested by Ben-Michael, to prevent the received data packets from being dropped when the on-chip memory of a router and/or switch is full. Kadambi does not disclose the eviction being based on an algorithm other than order of receipt in the first buffer. Brant discloses (col. 8 lines 50-54) an eviction algorithm other than the order of receipt such as random, revolving, least recently used or fastest fit algorithm. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include an eviction algorithm such as least recently used or fastest fit algorithm in Kadambi's system, as suggested by Brant, to efficiently manage the information units.

With respect to claims 2, 17, and 32 Kadambi discloses in Fig. 1, the forwarding element 10 is located on an IC chip (router processing is implemented on one or more router integrated circuit chips). As shown in Fig. 2, the CBP 50 is located inside of the SOC 10 on an IC chip (first set of buffers is located on the router integrated circuit chips). Further, as shown in Fig. 1, the external memory 12 is located off-chip (second set of buffers is located on memory chips separate from the router integrated circuit chips).

With respect to claims 3, 18, 33, and 41, Kadambi discloses (page 2, 13th paragraph) that packet length is estimated, based upon an incoming cell count and egress information, then it is determined whether external memory or internal memory is suitable to store the data packets (second set of buffers holds information units for a complete set of virtual channels).

With respect to claims 4, 19, 34, and 42, Kadambi disloses in Fig. 2 the CBP 50 is shared by all the ports (first set of buffer comprising a buffer pool shared by channels). Kadambi discloses (page 8, paragraph 109) that the free address pool within PMMU 70, Fig. 2, stores all free pointers for CBP 50. Each pointer in the free address pool points to a 64-byte cell in CBP 50 (a pointer array of pointers, associated with individual channels, to buffered information units).

With respect to claims 8-10, 23-25, 36-37, and 44, Kadambi, Ben-Michael and Brant have addressed all the claimed limitations recited in independent claim 1. Kadambi does not disclose flow control, such as blocking and/or credit-based, to stop the arrival of new information units while transferring information units between the first set of buffers and second set of buffers. Ben-Michael discloses (col. 2, lines 10-11) that credit based flow control is used to control the amount of data transmitted by a source node so that there is always a buffer available in the destination node to hold the data. Further, Ben-Michael discloses (see Abstract) that data is transferred to the off-chip memory when the on-chip memory is full. This means, by employing the credit based flow control, the source will hold its data while the data packets stored on-chip memory is offloaded to the off-chip memory, since no credits are being returned

upstream to notify the source that a buffer is available at the destination. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the flow control method in Kadambi's system, as suggested by Ben-Michael, to prevent the network from being congested when the on-chip memory of the received router is not available for accepting incoming data packets.

With respect to claims 11 and 26, Kadambi discloses (page 4, paragraphs 44-45, page 19, paragraphs 217-221, and Fig. 2) that the common buffer memory pool or CBP 50 is first level high speed SRAM memory, packet memory cache, for storing the received data packets and considered as on-chip data memory (a first set of rapidly accessible buffers, which store information units received at an input link). Further, Kadambi discloses that global memory buffer pool or GBP 60 acts as a second level memory and is located off-chip. Since, the GBP 60 is an off-chip memory therefore it is slower to access than the CBP 50 (a second set of buffers for the information units that are accessed more slowly that the first set). Kadambi does not disclose miss status registers to hold information units waiting for access to the second set of buffers. Ben-Michael discloses in Fig. 7, FIFO bank 1, considered by the examiner as miss status registers, storing and holding data packs for transferring to the off-chip memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include intermediate registers in Kadambi's system, as suggested by Ben-Michael, to hold the data packets before the off-chip memory is ready to accept the received data packets.

With respect to claims 12 and 27, Kadambi discloses (page 4, paragraphs 44-45, page 19, paragraphs 217-221, and Fig. 2) that the common buffer memory pool or CBP 50 is first level high speed SRAM memory, packet memory cache, for storing the received data packets and considered as on-chip data memory (a first set of rapidly accessible buffers, which store information units received at an input link). Further, Kadambi discloses that global memory buffer pool or GBP 60 acts as a second level memory and is located off-chip. Since, the GBP 60 is an off-chip memory therefore it is slower to access than the CBP 50 (a second set of buffers for the information units that are accessed more slowly that the first set). Kadambi does not disclose an eviction buffer to hold entries staged for transfer from the firs set of buffers to the second set of buffers. Ben-Michael discloses in Fig. 7, FIFO bank 1, considered by the examiner as an eviction buffer, storing and holding data packs for transferring to the off-chip memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the intermediate storage area in Kadambi's system, as suggested by Ben-Michael, to hold the data packets before the off-chip memory is ready to accept the received data packets.

With respect to claims 13 and 28, Kadambi discloses in Fig. 1, a forwarding element to be used in a local area communications networks (router is in a multi-computer interconnection network).

With respect to claims 14-15, 30, 38-39, and 45, Kadambi discloses in Fig. 2, the SOC is a forwarding element (router is a fabric router) and the received data packets are segmented into cells for storing and processing (information units are flits).

With respect to claims 50-53, Kadambi discloses in Fig. 2, the received data packets from the ports are stored in the CBP 50, processed and waited for its turn to transfer to the output port (means to arbitrate for plural information units to access an output channel).

With respect to claims 54-56, Kadambi discloses in Fig. 2, internal and external memories are shared memory among the input ports. Kadambi does not disclose separate buffer array of first and second set of buffers for each input port. However, it is well known in the art that each input port can have its separate memory for storing its received data packets. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include separate memory for each input port in Kadambi's system, for storing data received on its port and for not allocating its memory to other input ports even though other input ports may have higher received rates than its port.

3. Claims 5-7, 20-22, 35, and 43 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Kadambi et al (US Pub No. 2002/0093974 A1) in view of Ben-Michael et al (EP O 886454A2) and in view of Brant et al (US Patent No. 5,805,787) and further in view of the admitted prior art disclosed in the specification, page 7, lines 15-17 and Fig. 4.

With respect to claims 5-7, 20-22, 35, and 43, Kadambi discloses in Fig. 2, a high performance self-balancing low cost network switching architecture based on distributed hierarchical shared memory. Kadambi does not disclose first set of buffer is organized as a set-associative cache; wherein each entry in the set associative cache contains a single information unit; and wherein each entry in the set associative cache contains buffers and state for an entire virtual channel. The admitted prior art disclosed in the specification, page 7, lines 15-17 and Fig. 4, a set-associative cache, wherein each flit buffer is assigned to a particular virtual channel and held the information units in the flit buffers 204 and 205. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the feature of organizing the CBP 50 as a set-associative cache, in Kadambi's system, as suggested by the admitted prior art, to efficiently manage the received data packets in the shared memory.

Response to Arguments

4. Applicant's arguments filed March 22, 2004 have been fully considered but they are not persuasive.

Applicant argues on page 11 that Kadambi does not disclose or teach evicting packets from on-chip to off-chip memory. Examiner agrees. However, Kadambi was not relied upon for disclosing an eviction of packets from on-chip to off-chip memory. Instead, Kadambi discloses a data switch including a common buffer memory pool (first set of rapidly accessible buffers which store information units received at an input link) and a global memory buffer pool (second set of buffers for the information units that are accessed more slowly than the first set) for storing data received at the input ports.

Applicant argues on page 11 that the on-chip memory of the data switch of Kadambi does not function as a cache. Examiner respectfully disagrees. Kadambi discloses (page 4, paragraphs 44-45, page 19, paragraphs 217-221, and Fig. 2) that the common buffer memory pool or CBP 50 is first level high speed SRAM memory, packet memory cache (on-chip memory does function as a cache), for storing the received data packets and considered as on-chip data memory.

Applicant argues on page 12 that there would be no reason for one skilled in the art to combine the references. Examiner respectfully disagrees.

Kadambi discloses (page 1, 7th paragraph – page 2, 14th paragraph) that packets are buffered either to internal memory or external memory according to their lengths. Examiner recognized the fact that Kadambi does not disclose the information units, stored in the first set of buffers, being evicted to second set of buffers, when an overflow occurs in the first set of buffers. Therefore, Examiner has relied on Ben-Michael for teaching the eviction of packets from the on-chip memory to off-chip memory when an overflow occurs. Ben-Michael discloses in page 7, lines 41-42 that the FIFO may be used to store data packets (information units) rather than credits.

Ben-Michael discloses in Fig. 7, a block diagram illustrating on-chip memory and off-chip memory for storing data packets in a network switch or router, wherein, data packets being evicted from the on-chip memory to the off-chip memory when the on-chip memory is full.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the features of storing received data packets in the internal memory and transferring the received data packets to the external memory when an overflow

occurs in the internal memory of Kadambi's system, instead of determining where to buffer the received data packets, as suggested by Ben-Michael, to prevent the received data packets from being dropped when the internal memory of a router and/or switch is full. Further, it is reasonable to combine the teachings of Kadambi and Ben-Michael because both teach a way, a technique, a step, a process and/or a method on how to manage the received data packets in a switch/router of packet-based networks.

Applicant argues on page 12 that if one were to combine the two references as suggested by the Examiner, one would make use of the FIFO approach of Ben-Michael in the Kadambi reference, still failing to provide a cache with information units being evicted to second set of buffers according to an algorithm other than order of receipt in the first buffer. Examiner respectfully disagrees.

Examiner recognized the fact that in Ben-Michael reference, when an overflow occurs, the latest packets received at the input ports are transferred to the off-chip memory and then transferred back to the on-chip memory for transmissions out of the switch. Herein, let's say the latest packets are numbered as N1 ... Nn (N1 is the oldest arrival packet and Nn is the lastest arrival packet) and they are transferred in sequence of N1 to Nn to the off-chip memory. The important is to know where packets are stored in the memories.

Brant discloses (col. 8 lines 50-54) an eviction algorithm of packets other than the order of receipt such as random, revolving, least recently used or fastest fit algorithm. It is reasonable to combine the teachings of Brant and Ben-Michael and Kadambi because, some packets, ATM networks, are given a higher priority than other packets such as sensitive data, e.g., voice packets. Eventhough voice packets Nn arrive late at the switch inputs and an overflow occurs in

the on-chip memory, those voice packets can be queued in the first row of the external memory, since they are given a higher priority than a few packets arrived before them. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include an eviction algorithm such as least recently used or fastest fit algorithm in Kadambi's system, as suggested by Brant, to efficiently manage the data packets.

Even though the three references are from different application areas but they are all related on how to manage and transfer data packets between elements of a network or system.

Examiner has modified the rejection of claims 3, 18, 33, and 41 to clarify examiner's meaning. Kadambi discloses (page 2, 13th paragraph) that packet length is estimated, based upon an incoming cell count and egress information (virtual channel), then it is determined whether external memory (second set of buffers) or internal memory is suitable to store the data packets (second set of buffers holds information units for a complete set of virtual channels).

Applicant argues on page 14 that virtual channels and the problem of allocating buffer space for the virtual channels do not exist in ATM switch. Examiner respectfully disagrees but no further references are cited.

Applicant argues on page 14 that Ben-Michael discloses that credits are being transferred to the FIFO, not information units. Examiner respectfully disagrees, Ben-Michael discloses in page 7, lines 41-42 that the FIFO may be used to store data packets (information units) rather than credits.

Applicant argues on page 14 that from the description in Ben-Michael, the relationship between the FIFO banks 0 and 1 is not clear. However, FIFO bank 1 (considered, by the

examiner from the drawing, as miss status registers and/or eviction buffer), storing and holding data packs for transferring to the off-chip memory.

Applicant argues on pages 14-15 that the term "fabric router" is not the same as the forwarding element in Kadambi, as that term has been used in the present application. First of all, it is not part of the claimed invention. Secondly, it is unclear what is meant by the Applicant as "fabric router is a router that is within a large switch or router". At last, there is no difference between the forwarding element in Kadambi and fabric router

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H Ly whose telephone number is 703-306-5675. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 703-305-4378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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